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EXAMINER	
LESPERANCE, JEAN E	
ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/182,911	WILKS, BARRY G.	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8-28-2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-6,8,10-18,20-22,24-26,29,35-37,39 and 41-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-6,8,10-18,20-22,24-26,35-37,39 and 41-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The amendment filed on December 27, 2004 is entered and claims 4-6, 8, 10-18, 20-22, 24-26, 29, 35-37, 39, 41-49 are pending.

2. The indicated allowable subject matter of claims 13-18 and 29 is withdrawn and the rejection is provided below because of a 112 first paragraph (enablement) and a rejection is provided below.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 4-6, 8, 10-18, 20-22, 29, 44-47, and 49 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In independent claims 4, 8, and 20, the limitation "displaying at least a portion of the drawing surface on both of the multiple displays" is not described or mentioned anywhere in the specification. In independent claim 13, the limitations "first storage means, second storage means and third storage means" are not described anywhere in the

specification. Correction is required. The broadest interpretation will be used to reject the above claims with an art.

Claim Rejections - 35 U.S. C. § 103

4. The following is a quotation of 35 U. S. C. 103 (a), which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6, 8, 10-12, 20-22, 24-26, 29, 35-37, 39, 41-49 are rejected under 35 U.S.C. 102 (b) as being unpatentable over U.S. Patent # 4,990,902 ("Zenda") in view of U.S. Patent # 6,067,071 ("Kotha et al.").

Regarding claim 4, Zenda teaches a CRTC 13 receives a display timing signal parameter on system bus 3 in synchronism with display timing set command A supplied from CPU 1 through AND gate 15 (column 4, lines 11-14) corresponding to a) receiving display capability parameters regarding a first display of the multiple displays; the display timing signal generating parameters can be changed in correspondence with different display modes resolutions (column 2, lines 66-68) corresponding to b) substituting selected display capabilities of a second display of the multiple display for the received display capability parameters of the first display; and display resolution selecting means selects a display resolution (column 8, lines 43-44) corresponding to c) using the selected display capabilities of the second display with said first display; and then the power switch of the system is turned on, CPU 1 executes the display area control processing routine in BIOS 21 (column 4, lines 46-48) corresponding to wherein

step (a) further comprises receiving the capability parameters in accordance with a system start-up. Accordingly, Zenda teaches all the claimed limitations as recited in claims 4, 5, and 20 with the exception of providing the capability parameters comprise display resolution and display pixel depth.

However, Kotha et al. teach two video signals having different refresh rates and resolutions (column 5, lines 25-26) corresponding to a display refresh rate.

It would have been obvious to utilize video signals with different refresh rate as taught by Kotha et al. in the display area control system disclosed by Zenda because this would allow the display controller to output at least one of a plurality of different graphics display resolutions to a fixed resolution panel display.

Regarding claim 5, Zenda teaches a display resolution selecting means selects a display resolution (column 8, lines 43-44) corresponding to providing the selected display capabilities to an operating system; a display mode set command is input at keyboard 23 during execution of the application program, CPU 1 supplies display mode set command A to one input terminal of AND gate 15 through system bus 3, and executes the display mode set routine in BIOS 21. If it is determined in step 41 that the display mode is not altered, the flow advances to step 55, and CPU 1 executes initialization including clearing of V-RAM 9 (column 5, lines 4-12) corresponding to identify the capability parameters as primary parameters.

Regarding claim 6, Zenda teaches the display timing parameters must correspondingly be changed when a display screen is changed (column 3, lines 11 and

12) corresponding to receiving the capability parameters in response to a monitor change process.

Regarding claim 8, Zenda teaches a CPU Fig. 1 (1) corresponding to a processing module; and ROM Fig. 1 (5) corresponding to memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to a CRTC 13 receives a display timing signal parameter on system bus 3 in synchronism with display timing set command a supplied from CPU 1 through AND gate 15 (column 4, lines 11-14) corresponding to a) receiving capability parameters regarding a first display of the multiple displays; the display timing signal generating parameters can be changed in correspondence with different display modes resolutions (column 2, lines 66-68) corresponding to b) substituting selected display capabilities for the received capability parameters; and display resolution selecting means selects a display resolution (column 8, lines 43-44) corresponding to c) providing the selected display capabilities to an operating system; a display area control system for displaying on a flat panel display apparatus applied data generated by a desired application program, the display apparatus having the capability to display data corresponding to a plurality of different display resolutions (column 7, 8-13) corresponding to operational instructions that cause the processing module to determine the selected display capabilities based on a composite of the display parameters of each multiple displays.

Regarding claim 10, Zenda teaches When the power switch of the system is turned on, CPU 1 executes the display area control processing routine in BIOS 21

(column 4, lines 46-48) corresponding the memory further comprises operational instructions that causes the processing module to receive capability parameters in accordance with a system start-up and to monitor change process.

Regarding claim 11, Zenda teaches a display resolution selecting means selects a display resolution (column 8, lines 43-44) corresponding to providing the selected display capabilities to an operating system; a display mode set command is input at keyboard 23 during execution of the application program, CPU 1 supplies display mode set command A to one input terminal of AND gate 15 through system bus 3, and executes the display mode set routine in BIOS 21. If it is determined in step 41 that the display mode is not altered, the flow advances to step 55, and CPU 1 executes initialization including clearing of V-RAM 9 (column 5, lines 4-12) corresponding to identify the capability parameters as primary parameters.

Regarding claim 12, Zenda teaches When the power switch of the system is turned on, CPU 1 executes the display area control processing routine in BIOS 21 (column 4, lines 46-48) corresponding the memory further comprises operational instructions that causes the processing module to receive capability parameters in accordance with a system start-up and to monitor change process.

Regarding claim 13, Zenda teaches first memory means for storing a plurality of parameters for generating the different display timing signals in correspondence with a plurality of display resolutions (column 1, lines 56-59); second memory means for storing the parameter for generating the display timing signal read out from the first

memory means (column 1, lines 59-61) and ROM Fig.1 (5)read only memory stores parameters corresponding to the third memory means.

Regarding claim 14, Zenda teaches first memory means for storing a plurality of parameters for generating the different display timing signals in correspondence with a plurality of display resolutions (column 1, lines 56-59).

Regarding claim 15, Zenda teaches an application program, (note that an application program includes an operating system program hereinafter) developed for a CRT display (video graphics card) apparatus, is executed using a plasma display apparatus, if a designated display resolution is different from a currently set display resolution, a display timing signal generating parameter corresponding to the designated display resolution is set in a display timing register in a CRT controller. Thereafter, the content of the display timing register is inhibited from being changed until the execution of the application program is completed (column 2, lines 3-14).

Regarding claim 16, Zenda teaches an application program, (note that an application program includes an operating system program hereinafter) (system start-up) developed for a CRT display apparatus, is executed using a plasma display apparatus, if a designated display resolution is different from a currently set display resolution, a display timing signal generating parameter corresponding to the designated display resolution is set in a display timing register in a CRT controller. Thereafter, the content of the display timing register is inhibited from being changed until the execution of the application program is completed (column 2, lines 3-14).

Regarding claim 17, Zenda teaches a display resolution selecting means selects a display resolution (column 8, lines 43-44) corresponding to providing the selected display capabilities to an operating system; a display mode set command is input at keyboard 23 during execution of the application program, CPU 1 supplies display mode set command A to one input terminal of AND gate 15 through system bus 3, and executes the display mode set routine in BIOS 21. If it is determined in step 41 that the display mode is not altered, the flow advances to step 55, and CPU 1 executes initialization including clearing of V-RAM 9 (column 5, lines 4-12) corresponding to identify the capability parameters as primary parameters.

Regarding claim 18, Zenda teaches an application program, (note that an application program includes an operating system program hereinafter) developed for a CRT display apparatus, is executed using a plasma display apparatus, if a designated display resolution is different from a currently set display resolution, a display timing signal generating parameter corresponding to the designated display resolution is set in a display timing register in a CRT controller. Thereafter, the content of the display timing register is inhibited from being changed until the execution of the application program is completed.

Regarding claim 20, Zenda teaches a CRTC 13 receives a display timing signal parameter on system bus 3 in synchronism with display timing set command A supplied from CPU 1 through AND gate 15 (column 4, lines 11-14) corresponding to a) receiving display capability parameters regarding a first display of the multiple displays; the display timing signal generating parameters can be changed in correspondence with

different display modes resolutions (column 2, lines 66-68) corresponding to b) substituting selected display capabilities of a second display of the multiple display for the received display capability parameters of the first display; and display resolution selecting means selects a display resolution (column 8, lines 43-44) corresponding to c) using the selected display capabilities of the second display with said first display; and then the power switch of the system is turned on, CPU 1 executes the display area control processing routine in BIOS 21 (column 4, lines 46-48) corresponding to wherein step (a) further comprises receiving the capability parameters in accordance with a system start-up.

Regarding claim 21, Zenda teaches a display resolution selecting means selects a display resolution (column 8, lines 43-44) corresponding to providing the selected display capabilities to an operating system; a display mode set command is input at keyboard 23 during execution of the application program, CPU 1 supplies display mode set command A to one input terminal of AND gate 15 through system bus 3, and executes the display mode set routine in BIOS 21. If it is determined in step 41 that the display mode is not altered, the flow advances to step 55, and CPU 1 executes initialization including clearing of V-RAM 9 (column 5, lines 4-12) corresponding to identify the capability parameters as primary parameters.

Regarding claim 22, Zenda teaches the display timing parameters must correspondingly be changed when a display screen is changed (column 3, lines 11 and 12) corresponding to receiving the capability parameters in response to a monitor change process.

Regarding claim 24, Zenda teaches a CPU Fig. 1 (1) corresponding to a processing module; and ROM Fig. 1 (5) corresponding to memory operable coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to a CRTC 13 receives a display timing signal parameter on system bus 3 in synchronism with display timing set command a supplied from CPU 1 through AND gate 15 (column 4, lines 11-14) corresponding to a) receiving capability parameters regarding a first display of the multiple displays; the display timing signal generating parameters can be changed in correspondence with different display modes resolutions (column 2, lines 66-68) corresponding to b) substituting selected display capabilities for the received capability parameters; and display resolution selecting means selects a display resolution (column 8, lines 43-44) corresponding to c) providing the selected display capabilities to an operating system; a display area control system for displaying on a flat panel display apparatus applied data generated by a desired application program, the display apparatus having the capability to display data corresponding to a plurality of different display resolutions (column 7, 8-13) corresponding to operational instructions that cause the processing module to determine the selected display capabilities based on a composite of the display parameters of each multiple displays.

Regarding claim 25, Zenda teaches a display resolution selecting means selects a display resolution (column 8, lines 43-44) corresponding to providing the selected display capabilities to an operating system; a display mode set command is input at keyboard 23 during execution of the application program, CPU 1 supplies display mode

set command A to one input terminal of AND gate 15 through system bus 3, and executes the display mode set routine in BIOS 21. If it is determined in step 41 that the display mode is not altered, the flow advances to step 55, and CPU 1 executes initialization including clearing of V-RAM 9 (column 5, lines 4-12) corresponding to identify the capability parameters as primary parameters.

Regarding claim 26, Zenda teaches the display timing parameters must correspondingly be changed when a display screen is changed (column 3, lines 11 and 12) corresponding to receiving the capability parameters in response to a monitor change process.

Regarding claim 29, Kotha et al. teach To faithfully provide two distinct display resolutions, it may be desirable to generate two separate signals for two video displays having different resolutions, pixel depths, and/or refresh rates (column 4, lines 34-38).

As for claim 35, Kotha et al. teach the controller of the present invention uses a Discrete Time Oscillator (DTO) based clock divider and DCT based polyphase interpolation to upscale graphics display data from a first resolution to the panel resolution (abstract) corresponding to a display with a video graphic card. It is well known in the art to have a graphic display there must exist a video graphic card.

Regarding claim 36, Zenda teaches a display resolution selecting means selects a display resolution (column 8, lines 43-44) corresponding to providing the selected display capabilities to an operating system; a display mode set command is input at keyboard 23 during execution of the application program, CPU 1 supplies display mode set command A to one input terminal of AND gate 15 through system bus 3, and

executes the display mode set routine in BIOS 21. If it is determined in step 41 that the display mode is not altered, the flow advances to step 55, and CPU 1 executes initialization including clearing of V-RAM 9 (column 5, lines 4-12) corresponding to identify the capability parameters as primary parameters.

Regarding claim 37, Zenda teaches the display timing parameters must correspondingly be changed when a display screen is changed (column 3, lines 11 and 12) corresponding to receiving the capability parameters in response to a monitor change process.

Regarding claim 39, Zenda teaches a CPU Fig. 1 (1) corresponding to a processing module; and ROM Fig. 1 (5) corresponding to memory operable coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to a CRTC 13 receives a display timing signal parameter on system bus 3 in synchronism with display timing set command a supplied from CPU 1 through AND gate 15 (column 4, lines 11-14) corresponding to a) receiving capability parameters regarding a first display of the multiple displays; the display timing signal generating parameters can be changed in correspondence with different display modes resolutions (column 2, lines 66-68) corresponding to b) substituting selected display capabilities for the received capability parameters; and display resolution selecting means selects a display resolution (column 8, lines 43-44) corresponding to c) providing the selected display capabilities to an operating system; a display area control system for displaying on a flat panel display apparatus applied data generated by a desired application program, the display apparatus having the capability to display data

corresponding to a plurality of different display resolutions (column 7, 8-13) corresponding to operational instructions that cause the processing module to determine the selected display capabilities based on a composite of the display parameters of each multiple displays.

Regarding claim 41, Zenda teaches When the power switch of the system is turned on, CPU 1 executes the display area control processing routine in BIOS 21 (column 4, lines 46-48) corresponding the memory further comprises operational instructions that causes the processing module to receive capability parameters in accordance with a system start-up and to monitor change process.

Regarding claim 42, Zenda teaches a CRTC 13 receives a display timing signal parameter on system bus 3 in synchronism with display timing set command A supplied from CPU 1 through AND gate 15 (column 4, lines 11-14) corresponding to a) receiving display capability parameters regarding a first display of the multiple displays; the display timing signal generating parameters can be changed in correspondence with different display modes resolutions (column 2, lines 66-68) corresponding to b) substituting selected display capabilities of a second display of the multiple display for the received display capability parameters of the first display; and display resolution selecting means selects a display resolution (column 8, lines 43-44) corresponding to c) using the selected display capabilities of the second display with said first display; and then the power switch of the system is turned on, CPU 1 executes the display area control processing routine in BIOS 21 (column 4, lines 46-48) corresponding to wherein

step (a) further comprises receiving the capability parameters in accordance with a system start-up.

Regarding claim 43, Zenda teaches the display timing parameters must correspondingly be changed when a display screen is changed (column 3, lines 11 and 12) corresponding to receiving the capability parameters in response to a monitor change process.

As for claim 44, Zenda teaches a display resolution selecting means selects a display resolution which differs from the display resolution corresponding to the designated set of display timing signal generating parameters, and when the predetermined number of picture elements in the horizontal direction of the selected display resolution is smaller than the maximum number of picture elements in the horizontal direction, said control means generates display timing signals so that non-display areas having picture elements which number a difference between the predetermined and maximum numbers of picture elements in the horizontal direction are formed on the right and left portions of the physical screen of the flat panel display apparatus (column 8, lines 58-68) corresponding to capability parameters that exceed the display parameters of each of the multiple displays. It means that the selected display capability parameters is twice the display parameters of each of the multiple

Regarding claim 45, Zenda teaches display timing signal generating parameters (PD) having display timings for forming upper and lower non-display areas of 25 dots, as shown in FIG. 2B, are read out from ROM 5, and are set in display timing register 14 of CRTC 13 through system bus 3. As a result, CRTC

13 generates display timing signals based on input parameters PD, and supplies the signals to plasma display apparatus 7 through pallet 11 (column 5, lines 67 and 69 and column 6, lines 1-7).

Regarding claim 46, Zenda teaches display timing signal generating parameters (PD) having display timings for forming upper and lower nondisplay areas of 25 dots, as shown in FIG. 2B, are read out from ROM 5, and are set in display timing register 14 of CRTC 13 through system bus 3. As a result, CRTC 13 generates display timing signals based on input parameters PD, and supplies the signals to plasma display apparatus 7 through pallet 11 (column 5, lines 67 and 69 and column 6, lines 1-7).

Regarding claim 47, Zenda teaches display timing signal generating parameters (PD) having display timings for forming upper and lower nondisplay areas of 25 dots, as shown in FIG. 2B, are read out from ROM 5, and are set in display timing register 14 of CRTC 13 through system bus 3. As a result, CRTC 13 generates display timing signals based on input parameters PD, and supplies the signals to plasma display apparatus 7 through pallet 11 (column 5, lines 67 and 69 and column 6, lines 1-7).

Regarding claim 48, Zenda teaches display timing signal generating parameters (PD) having display timings for forming upper and lower nondisplay areas of 25 dots, as shown in FIG. 2B, are read out from ROM 5, and are set in display timing register 14 of CRTC 13 through system bus 3. As a result, CRTC 13 generates display timing signals based on input parameters PD, and supplies

the signals to plasma display apparatus 7 through pallet 11 (column 5, lines 67 and 69 and column 6, lines 1-7).

Regarding claim 49, Zenda teaches display timing signal generating parameters (PD) having display timings for forming upper and lower nondisplay areas of 25 dots, as shown in FIG. 2B, are read out from ROM 5, and are set in display timing register 14 of CRTC 13 through system bus 3. As a result, CRTC 13 generates display timing signals based on input parameters PD, and supplies the signals to plasma display apparatus 7 through pallet 11 (column 5, lines 67 and 69 and column 6, lines 1-7).

Response to Amendment

5. Applicant's arguments filed on December 27, 2004 have been fully considered but they are not persuasive. The applicant argued that the quote in page 4, lines 27-30, "each of the displays may be driven from the drawing surface such that they each display the same image" is the same as "displaying at least a portion of the drawing surface on both of the multiple displays". Examiner disagrees with the applicant that the two above quotes are the same. They are very different. The 112 first paragraph is maintained. Applicant argued that the prior art, Zenda and Kotha et al, fail to teach outputting on multiple displays at the same time. Examiner disagrees because Kotha et al. teach a control Logic 304 may store values corresponding to fixed display resolution and desired display resolution. By making values for fixed resolution and desired resolution settable in registers, output resolution is decoupled from a hardware

implementation in core logic. Rather than write complex drivers on an individual basis for each display likely to be encountered, developers may simply set values in registers to drive displays of many types including fixed resolution displays. Applicant argued that the prior arts, Zenda and Kotha et al. fail to teach displaying the same display or drawing surface on multiple displays at the same time as multiple display output. Examiner disagrees with the applicant because Kotha et al. teach When such multimedia display equipment is used with conventional portable computers, because of fixed resolution related problems, a single display resolution only may be displayed on both displays (internal or projected) at the same time (column 4, lines 6-10) corresponding to displaying the same display or drawing surface on multiple displays at the same time as multiple display output. Therefore the rejection is maintained.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (571) 272-7692. The examiner can normally be reached on from Monday to Friday between 8:OOAM and 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard, can be reached on (571) 272-7603.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only

Hand-delivered responses should be brought to Crystal Park 11, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art Unit 2674

Date 5/17/2005

HENRY N. TRAN
PRIMARY EXAMINER